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An approach for broadband modem FIR filter design optimization is presented. It addresses the minimization of the number of adder-subtractors used in the hardware implementation of a FIR filter (Multiple Constant Multiplication problem). The method is based on identification and elimination of n-bit pattern common subexpressions in a set of filter coefficients by means of an exhaustive search. We give an algorithm description of our solution and demonstrate the performance on selected examples
3 Low power multiplication for FIR filters  Chris J. Nicol, Patrik Larsson August 1997 Proceedings of the 1997 international symposium on Low power electronics and design  Full text available: pdf(473.68 KB) Additional Information: full citation, references, citings
4 Session 11: A low power normalized-LMS decision feedback equalizer for a wireless  packet modem David Garrett, Chris Nicol, Andrew Blanksby, Chris Howland August 2002 Proceedings of the 2002 international symposium on Low power

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This paper presents a decision feedback equalizer (DFE) for a high-speed packet modem utilizing the normalized least mean squared (NLMS) tap update algorithm. The equalizer supports up to 43.2 Mbps uncoded data over a wireless channel with a 10% training preamble (48 Mbps with no training). In this work the rapid convergence of the NLMS algorithm is combined a technique for early termination of the tap training process to yield a low power DFE implementation. The low power techniques result in a ...

Keywords: NLMS, early termination, equalization, low power

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	<u>modern</u> Hyeongseok Yu, Byung Wook Kim, Yeon Gon Cho, Jun-Dong Cho, Jea Woo Kim, Hyun Cheol	

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In this paper, an area efficient VLSI architecture of decision feedback equalizer is derived accommodating 64/256 QAM modulators. This architecture is implemented efficiently in reusable VLSI structure using EDA tool due to its regular structure. The main idea is to employ a time-multiplexed design scheme grouping the adjacent filter taps with correlated internal dataflow and with data transfer having same processing sequence between blocks. We simulated the proposed design scheme using SYN ...

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